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EXAMINER	
FIEGLE, RYAN PAUL	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/030,106	MERCK, MARTIN	
	Examiner	Art Unit	
	Ryan P. Fiegle	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The new title is sufficient and accepted.

Drawings

2. The replacement drawing sheet is accepted.

Claim Objections

3. The examiner thanks the applicant for amending claim 14 to better state what was meant by the applicant.

4. The objection to claim 17 is upheld. In claim 12, it states that the operand stack is for a calculating machine. The presence of the calculating machine is inherent since the operand stack would not be of much use without it. Therefore, claim 17 fails to further limit its base claim.

Response to Arguments

5. The applicant has made the following argument:

> "Nowhere in the Morris patent is there a disclosure of storing operands of different lengths in a stack having variable length elements."

The examiner acknowledged in his office action that Morris does not teach storing operands of different lengths in a stack having variable length elements. This is why the combination was made with Shibasaki.

6. The applicant has made the following argument:

> "In fact, the whole point of the device in the Morris patent is to create data units having uniform word sizes to ease processing. This is in direct contrast to the pending claims, which allow processing to occur with operands of variable length."

The applicant is arguing a feature not specifically stated in the claim language, which is improper. Claimed subject matter, **not** the specification, is the measure of invention. Limitations in the specification **cannot** be read into the claims for the purpose of avoiding the prior art. *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978).

> *It is the claims that measure the invention." SRI Int'l v. Matshshita Elec. Corp., 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).*
>
> *"The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." In re Hiniker Co., 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).*
>
> *"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." In re Morris, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).*
>
> *"limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be **confused with adding an extraneous limitation** appearing in the specification, which is improper'." Intervet Am., v. Kee-Vet Labs., 12 USPQ2d 1474, 1476 (Fed. Cir. 1989) (citation omitted).*
>
> *"it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is **not*** to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." In re Paulsen, 31 USPQ2d 1671, 1674 (Fed. Cir. 194) (citation omitted).
>
> *"[A]n examiner has the duty to police claim language by giving it the broadest reasonable interpretation." Springs Window Fashions LP v. Novo Industries L.P., 65 USPQ2d 1826, 1930 (Fed. Cir. 2003).*

7. The applicant has made the following argument:

> "The Morris patent further does not disclose a type memory for storing coded type information corresponding to each operand."

The cited section, column 6, lines 38-41, refers to a length of an operand that the applicant claims does not disclose type information. The examiner believes length to be a type. For example, 4 bits is a nybble, 8 bits is a byte, and so on.

8. The applicant has made the following argument:

> "The whole system in the Morris patent is based upon the use of a "1-word" register. This is an essential portion of the system of the Morris patent, and one of ordinary skill in the art would not be motivated to replace the "l-word" register with the stack of uniform operand elements disclosed by the Shibasaki et al. patent.
>
> "Replacing the "1-word" register in the Morris patent with the stack disclosed by the Shibasaki et al. patent would require many tedious modifications in structure, as well as in command programming, to the system of the Morris patent. Such extensive modifications would deter, rather than motivate, one of ordinary skill in the art from making the suggested change."

The examiner disagrees. As discussed in the previous office action, memory-memory processors have absolutely no place in modern computing. Memory latencies are incredibly inhibiting to modern processors, and it the goal of every designer to keep them to an absolute minimum.

Therefore, one of ordinary skill in the pertinent art **at the time of the applicant's invention** would have been motivated to do ***anything*** to prevent a modern implication of Morris to preclude the use of the "1-word" register, including totally redesigning the data path.

However, replacing one temporary storage system with another is not very difficult. In the case of the combination of Morris and Shibasaki, the end result would greatly simplify the system. This doesn't even include the numerous other advantages listed in the previous office action and below, as well as in Shibasaki.

Therefore, the examiner believes that there is ample motivation to combine Morris and Shibasaki.

9. The applicant has made the following argument:

> "Therefore, there is no reasonable expectation that the combination of the Morris patent and the Shibasaki et al. patent would successfully disclose every limitation of the pending claims."

Considering the broad limitations of the claims, the examiner does not believe this to be the case.

Further, the implication of an operand stack is very well known in the art, and therefore the examiner believes it would not be difficult to apply it to another system to produce the claimed results.

10. The applicant has made the following argument:

> "With regards to claim 13, the rejection states that it would have been obvious to have a type memory formed in a stack with constant length, since the type memory must keep a one-to-one relationship with the operand stack. The rejection provides no evidence or support for this conclusionary statement."

In Morris, each operand contains length information kept in the length register. The same motivation would be used to make the length register a stack as was used to make the operand register a stack. Memory accesses impede a processor. If an operand stack is present in the processor, but it cannot be accessed quickly because the processor does not know the length of the TOS without first loading the length of the TOS from memory, then it is not of much use. The processor must quickly be able to know the length of the top element, and thus the length register must also be implemented as a stack in the combination of Morris and Shibasaki.

11. The applicant has made the following argument:

> "With regards to claim 14, the rejection states that it would have been obvious to integrate the type memory and the operand memory, since "it makes the most sense" to do so. The rejection further states that this is done in communication theory. However, the rejection provides no evidence or support for these conclusionary statements."

Sanders (US Patent 4,135,156) discloses a packet header with a packet length (column 8, lines 65-68; column 9, lines 1-5).

12. The applicant has made the following argument:

> "With regard to claim 15, the rejection asserts that it would have been obvious to form the operand memory stack having variable length operands as a virtual stack in a virtual calculating machine, since virtual stacks are well known in the art. The rejection provides no evidence of virtual stacks having variable length operand elements."

Making the operands on a stack variable length does not affect the implementation of the stack itself, i.e. it is still a LIFO structure that pushes and pops elements. Implementations of virtual stacks are well known, and since it has been shown through the combination of Morris and Shibasaki that a stack with variable length operands can be implemented, implementing the combination of Morris and Shibasaki as a virtual stack would be an obvious variation.

13. The applicant has made the following argument:

> "With regard to claim 16, the rejection broadly asserts that error checking for length is well known in the art, but provides no evidence of specifically checking the operand type at each read access to the operand memory stack."

Smolko (US Patent 4,213,188) discloses a type error check for operands (Smolko: column 9, lines 36-38). Checking for length error is also well known as seen in Gunzberg (US Patent 4,408291) (Gunzberg: column 23, lines 29-35). One of ordinary skill in the pertinent art at the time of the applicant's invention would have recognized that when data is not a static length, the length must be checked before it is used. This is a common idea in communication, and would carry over to architecture.

14. The applicant has made the following argument:

> "Here, the rejection fails to establish that the device of the pending claim is old, as discussed above, and therefore, it is a patentable feature to make the device of the pending claims portable."

For the reasons discussed above, and in the rejections below, the examiner believes the invention to be old at the time of the applicant's invention, and therefore portability is not a patentable feature.

Further, the applicant argues that applying the invention to a smart card would modify the structure of the device. The examiner respectfully disagrees. Since this device would be implemented on the nanometer level, the examiner fails to see how the structure would need to be changed to be implemented in a smart card. In addition, these changes are not covered within the specification, let alone the claims.

Claim Rejections - 35 USC § 103

15. The examiner has reviewed the amendments to the claims and acknowledges that they do not add new matter or change the scope of the invention. Therefore, new grounds of rejection are not necessitated and the same rejections used in the previous office action have been inserted below as reference.

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 12-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Morris (US Patent 3,873,976) in view of Shibasaki et al. (US Patent 4,334,269).

18. As per claim 12:

Morris teaches a storage means (Morris: Figure 1, item 118) for a calculating machine containing a processing unit processing individual operands according to a program (Morris: column 2, lines 48-53), and

the storage means in which operands of different lengths are stored (Morris: column 1, lines 42-48), characterized by a type memory filled with a type indicator of constant length which stores for each operand stored in the storage means its type information which contains information about the length of the relevant operand (Morris: column 6, lines 38-41),

the length of the particular operand type being stored in a table in dependence on the corresponding type code (Morris: column 6, lines 38-41) (Since the content of the length register corresponds to the storage capacity, it is inherent that the length of the particular operand type being stored in the length register is in dependence on the type code, which also happens to be the value kept in the length register).

Morris does not teach his storage means being a stack. In fact, Morris does not disclose any temporary storage short of the data register (Morris: Figure 1, item 118). One of ordinary skill in the pertinent art would have recognized that this is not sufficient for normal program computing since most operations contain at least two operands. Though an accumulator could possibly be used, it is not optimum since it requires many memory accesses. If Morris were to be used in modern designs at the time of the applicant's invention, it should not be bogged down by constant memory accesses since memory accesses inhibit modern processors.

Shibasaki discloses that a stack processor has the advantage of not having to save and store data on a context switch because new values created in the new context are just pushed on top of the old ones (Shibasaki: column 1, lines 39-44). In addition, stack-based compilers are usually simpler than register-based compilers (Shibasaki: column 1, lines 44-51).

Therefore, one of ordinary skill in the pertinent art at the time of the applicant's invention would have recognized that utilizing an operand stack as temporary storage in Morris would provide the benefit of completing instructions with two or more operands, avoiding constant memory accesses, not having to backup temporary storage during a context switch and providing a simpler compiler.

In addition, Shibasaki provides the added benefit of combining a stack-based processor and a register-based processor to increase throughput and simplify the instruction set (Shibasaki: column 3, lines 67-68; column 4, lines 1-6). However, it should be noted that Shibasaki's design would not be mandatory since stack-based processors are well and known in the art (see King) and the benefits listed in Shibasaki would remain true for all stack-based processors.

19. As per claim 13:

An operand stack according to claim 12, characterized in that the type memory is formed as a stack with constant length stack elements separate from the operand memory (Morris: Figure 1, items 118 and 124) (From the figure it can be seen that they are separate).

It would have been obvious to one of ordinary skill in the pertinent art that the length register would also have to be applied as a stack since it must keep a 1-to-1 relationship with the operand stack.

20. As per claim 14:

An operand stack according to claim 12, characterized in that the type memory is integrated operand by operand into the operand memory (Morris: column 8, lines 1-5).

Morris does not disclose where the length is taken from to load into the length register, which when combined with Shibasaki would become the length stack. However, one of ordinary skill in the pertinent art would have recognized that it would make the most sense to integrate it in with the operands. Separating the operands and the length fields would mean a very complex data fetching scheme as well as limiting the potential data space. Taking an example for communication theory, the length of each packet is contained in the header of a packet rather than at the end of a total transmission or a totally separate transmission on another port. Such is done for coherency and error correction. The same concepts would remain true when applied to Morris' scheme.

21. As per claim 15:

An operand stack according to claim 12, characterized in that the operand stack is formed as a virtual stack for a virtual calculating machine.

Virtual stacks are very well known in the art. King, as aforementioned, keeps the majority of his stack as a virtual stack in memory. Virtual call stacks for routine calls are very well known in the art. Further, virtual operand stacks in Java virtual machines are

very well known in the art. Therefore, it would have been obvious to apply the operand stack as a virtual stack in a virtual calculating machine (Official Notice).

22. As per claim 16:

An operand stack according to claim 12, characterized by an operand type-checking device which is activated at each read access to the operand memory.

Error checking for length is well known in the art. Mechanisms such as parity and counting the number of received bytes by a length field received in a header are well established. Such would have been obvious to apply to Morris since the operands are coming from I/O and peripherals (Morris: column 1, lines 58-63) (Official Notice).

23. As per claim 17:

A calculating machine having an operand stack according to claim 12 (Morris: column 2, lines 48-53).

24. As per claim 18:

A smart card having an integrated virtual calculating machine according to claim 12.

Putting the operand stack on a smart card would at most make it portable, which has been found in In re Lindberg (194 F.2d 732, 735, 93 USPQ 23, 26 (CCPA 1952)) to not be a distinguishing patentable feature.

25. As per claim 19:

Claim 19 is the method claim of claim 12 containing the same limitations. Since it is inherent that the system designed to perform the method would also teach the method, claim 19 is rejected for the same reasons as claim 12.

26. As per claim 20:

Claim 20 is the method claim of claim 13 containing the same limitations. Since it is inherent that the system designed to perform the method would also teach the method, claim 20 is rejected for the same reasons as claim 13.

27. As per claim 21:

Claim 21 is the method claim of claim 14 containing the same limitations. Since it is inherent that the system designed to perform the method would also teach the method, claim 21 is rejected for the same reasons as claim 14.

28. As per claim 22:

Claim 22 is the method claim of claim 16 containing the same limitations. Since it is inherent that the system designed to perform the method would also teach the method, claim 22 is rejected for the same reasons as claim 16.

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

30. Sanders (US Patent 4,135,156) discloses a packet header with a packet length.

31. Smolko (US Patent 4,213,188) discloses a type error check for operands.

32. Gunzberg (US Patent 4,408291) teaches length error detection.

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan P. Fiegle whose telephone number is 571-272-5534. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ryan P Fiegle
Examiner
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